Free-of-Charge Libraries

Artisan 0.18um Library

Standard Cell

- 478 high-density standard cells
- 9-track cell architecture
- Average cell density of 111K gates/sq.mm
- Multiple drive strengths
- Routable in 3, 4, 5 or more metal layers
- Comprehensive design tool support
- Process specific electrical and physical tuning

Single Port and Dual Port SRAM Compilers

- Exceptional speed
- Broadly configurable
- Low active power and leakage-only standby current
- Complete set of tool models and characterization data
- Flexible power routing
- Zero hold time (data, address and control inputs)

Inline I/O

- 600+ 3.3V/5VT
- Pad pitch: 60 um
- Input: pull-up/pull-down, Schmitt trigger, LVTTL, CMOS
- Output: multiple current up tp 24mA with 3 slew rate options
- Special pads: clock, crystal oscillator, corner, power and ground

Architecture	Word	Bit	Mux	Size	Access Time (ns)
Single Port Sync. SRAM	16 - 8K (Increment: 2X mux)	2 - 128 (Increment: 1)	4, 8, 16	32 bit - 512 Kbit	4K x 16 Typical: 1.21 Worst: 2.13
Dual Port Sync. SRAM	16 - 8K (Increment: 2X mux)	2 - 128 (Increment: 1)	4, 8, 16	32 bit - 512 Kbit	4K x 16 Typical: 1.28 Worst: 2.26

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Free-of-Charge Libraries

Virtual Silicon 0.18um Library

Standard Cell

- 500+ high performance standard cells
- 11-track cell architecture, performance optimized for 200~700 MHz
- Average cell density of 90K gates/sq.mm
- Multiple drive strengths
- Layout using metal 1 only
- Scan version of every flip-flop available
- Fully contacted well ties
- Accurate modeling and characterization for timing and power
- Open architecture developers kit available

Inline and Staggered I/O

- 700+ 3.3V & 3.3V/5VT I/O pads
- Pad pitch: 60um (In-line), 40um (Staggered)
- Multiple current drives up to 24mA
- Input: Pull-up/pull-down resistor, pad keeper, normal/ Schmitt
- Output and bi-directional with slew rate control
- Silicon proven ESD and latch-up structures
- Analog power pads, crystal pads
- Open architecture developers kit available

PLL Compilers

- Programmable input, output frequencies and duty cycle
- Input frequency range: 20 MHz - 200 MHz
- Output frequency range: 50MHz -900MHz
- PLL module entirely located in the I/O pad rings
- Dedicated analog power supply pins
- Build-in ESD and latch-up protection structures

Single Port Synchronons SRAM and Two Port Register File Compilers

- Synchronous reads/writes
- Static design with zero standby current
- Byte write capability
- Routable over the core with higher metal layer
- Ability to compile to multiple aspect ratio
- Scan and BIST support

Architecture	Word	Bit	Mux	Size	Access Time (ns)
Single Port Sync. SRAM	32 - 4K (Increment: 2X mux)	2 - 128 (Increment: 1)	2, 4, 8, 16	32 bit - 256 Kbit	4K x 16 Typical: 1.80 Worst: 3.36
Two Port Register File	8 - 1K (Increment: 2X mux)	4 - 128 (Increment: 1)	1, 2, 4	32 bit - 64 Kbit	128K x 64 Typical: 1.37 Worst: 2.38

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Free-of-Charge Libraries

Faraday 0.18um GII Library

Standard Cell

- 400+ high performance standard cells
- 9-track cell architecture
- Average cell density >120K gates/sq.mm
- Optimized multiple drive strengths
- High porosity and routability
- Scan version of every flip-flop available
- Ultra low power cell available
- Gated input for preventing leakage
- Fully tool models support

Single Port SRAM, Dual Port SRAM, One Port Register File, Two Port Register File, and Via2 ROM Compilers

- Synchronous reads/writes
- Static design with zero standby current
- Byte write capability
- Provides both high speed and low power SRAMs
- Ability to compile to multiple aspect ratio
- Scan and BIST support
- Power port connections support
- Zero hold time for inputs

Inline and Staggered I/O

- 1.8V, 3.3V I/O pads
- 1.8V/2.5VT, 3.3V/5VT I/O pads
- Support over 500+ IO Functions
- Pad pitch: 65um (In-line), 40um (Stagger)
- Programmable current drives and slew rate control from 2mA to 16mA
- Programmable pull-up/pull-down resistor, normal/ Schmitt trigger
- Provide 90+ programming features in one I/O
- In-line to staggered I/O corner available

Architecture	Word	Bit	Mux	Size	Access Time (ns)
Single Port Sync. SRAM	64 - 64K (Increment: 16 x mux)	1 - 128 (Increment: 1)	1, 2, 4, 8, 16	64 bit - 512 Kbit	4K x 16 Typical: 1.80 Worst: 3.1
Single Port Sync. Register File	32 - 2K (Increment: 2 x mux)	1 - 144 (Increment: 1)	2, 4, 8	32 bit - 72 Kbit	1K x 16 Typical: 1.63 Worst: 2.72
Dual Port Sync. SRAM	64 - 32K (Increment: 16 x mux)	1 - 128 (Increment: 1)	1, 2, 4, 8	64 bit - 512 Kbit	4K x 16 Typical: 1.80 Worst: 3.1
Two Port Sync. Register File	4 - 2K (Increment: 2 x mux)	2 - 144 (Increment: 1)	2, 4, 8	8 bit - 72 Kbit	1K x 64 Typical: 1.7 Worst: 2.8
Via2 ROM	128 - 128K (Increment:128 x mux)	1 - 128 (Increment: 1)	1, 2, 4 ,8	128 bit - 2 Mbit	4K x 16 Typical: 2 Worst: 3.4

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Free-of-Charge Libraries

Faraday 0.18um LL Library

Standard Cell

- 400+ high performance standard cells
- 9-track cell architecture
- Average cell density >120K gates/sq.mm
- Optimized multiple drive strengths
- High porosity and routability
- Scan version of every flip-flop available
- Ultra low power cell available
- Gated input for preventing leakage
- Fully tool models support

Single Port SRAM, Dual Port SRAM, Two Port Register File and Via1 ROM Compilers

- Synchronous reads/writes
- Static design with zero standby current
- Byte write capability
- Provides both high speed and low power SRAMs
- Ability to compile to multiple aspect ratio
- Scan and BIST support
- Power port connections support
- Zero hold time for inputs

Inline and Staggered I/O

- 1.8V, 3.3V I/O pads
- 1.8V/2.5VT, 3.3V/5VT I/O pads
- Support over 500+ IO Functions
- Pad pitch: 65um (In-line), 40um (Stagger)
- Programmable current drives and slew rate control from 2mA to 16mA
- Programmable pull-up/pull-down resistor, normal/
- Schmitt trigger
- Provide 90+ programming features in one I/O
- In-line to staggered I/O corner available

Architecture	Word	Bit	Mux	Size	Access Time (ns)
Single Port Sync. SRAM	64 - 64K (Increment: 16 x mux)	1 - 128 (Increment: 1)	1, 2, 4, 8, 16	64 bit - 512 Kbit	4K x 16 Typical: 2.7 Worst: 4.6
Dual Port Sync. SRAM	64 - 32K (Increment: 16 x mux)	1 - 128 (Increment: 1)	1, 2, 4, 8	64 bit - 512 Kbit	4K x 16 Typical: 2.80 Worst: 4.8
Two Port Sync. Register File	1 - 2K (Increment: 1 x mux)	1 - 144 (Increment: 1)	1, 2, 4, 8	1bit - 36 Kbit	1K x 16 Typical: 4.7 Worst: 8
Via1 ROM	256 - 128K (Increment:256 x mux)	1 - 128 (Increment: 1)	1, 2, 4 ,8	256 bit - 2 Mbit	4K x 16 Typical: 3.8 Worst: 6.6

Non-Free Libraries

Virage Logic 0.18um Memory Compiler

	HJTC Process Type	Word Width (bits/word)	Word Depth (words)	Max Size (Kbits)	Max Configuration	Aspect Ration (Yes/NO)	Bit/Byte write capability	Redundancy Built-in
SP HD SRAM	GII	2 - 128	16 - 16K	32 - 512K	16Kx32	Yes: 4,8,16	Yes	No
DP HD SRAM	GII	2 - 128	16 - 8K	32 - 256K	8Kx32	Yes: 4,8,16	Yes	No
2P Register File	GII/LL	2 - 256	8 - 1024	16 - 16K	1Kx16	Yes: 1,2,4	Yes	No
ROM	GII/LL	8 - 64	256 - 64K	2K - 1M	64Kx16	Yes: 16,32,64	No	No
SP HS SRAM	GII/LL	2 - 256	16 - 16K	32 - 512K	16Kx32	4,8,16	Yes	No
DP HS SRAM	GII/LL	2 - 256	32 - 8K	64 - 256K	8Kx32	4,8,16	Yes	No
SP STAR HD-4M(SRAM with redundancy)	GII	8 - 256	128 - 64K	16K - 4M	64Kx64	Yes: 8,16,32	Yes	Yes
SP STAR HS-512K(SRAM with redundancy)	GII	2 - 256	16 - 16K	32 - 512K	16Kx32	4,8,16	Yes	Yes
DP STAR HS-512K(SRAM with redundancy	GII	2 -256	32 - 8K	64 - 256K	8Kx32	4,8,16	Yes	Yes
T-CAM 32K	GII	16 - 64	16 - 512	1K - 32K	512Kx64	1	No	No

Artisan 0.18 um Library

Standard I/O

- 1000+ High Performance standard cells
- 9-track cell architecture
- Average cell density of 73K gates/sq.mm
  Multiple drive strengths
- Silicon proven
- Scan version of every flip-flop available
- Compatible with mixed signal environment
- Accurate timing and power models

In-line and staggered I/O

- 3.3V/5VT
- Pad pitch: 76.8um (In-line), 38.4um (Staggered)
- Multiple current drives up to 16mA
- Pull ups, Pull downs, switchable
- Hysteresis
- Built-in level shifting