EE Solutions

HeJian

DATASHEET

HEJIAN-EES REFERENCE DESIGN FLOW

Executive Summary

EE Solutions and HeJian have developed and verified an open source reference design based on **HeJian's 0.18um** processing technology. Different views of the reference design were created using a mixture of Cadence, Synopsys, and Mentor tools. The set of tools were chosen as a foundation to establish HeJian's Reference Design Flow. The flow can also be enhanced to add new capabilities in the near future. The current release of the Reference Design Flow is a verified and silicon proven design flow. It provides a guided design creation from RTL to GDSII based on HeJian's 0.18um process technology. The design tools that are used for implementing the design flow including Synopsys Design Compiler™, Cadence SoC Encounter™, Synopsys PrimeTime™, Cadence NC-Verilog Simulator™, Cadence VoltageStorm™, Cadence Fire&Ice QXC™, and Mentor Graphics Calibre™. The libraries that were used throughout the design steps included both Artisan's I/O cell and Artisan's Standard Cell libraries.

The initial objective for the joint partnership is to use HeJian's Reference Design Flow as a guideline to solve the following design problems:

- **Timing Closure**
- **Power Integrity**

Future design capabilities will be added pending upon customer request. You can refer to the reference design flow and apply the selected tools in each step of the design flow to generate the desired GDSII file.

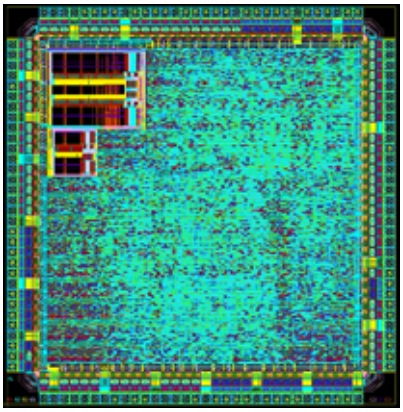

Figure 1: Decoding/Encoding Accelerator is implemented and verified using HeJian Reference Design Flow at 0.18um process technology.

HeJian Reference Design Flow

HeJian's Reference Design Flow provides a predictable path to silicon and offers a better control for the project schedule. This design flow enables on-time design completion that meets timing constraints and takes into account the deep-sub-micron effects such as IR drop.

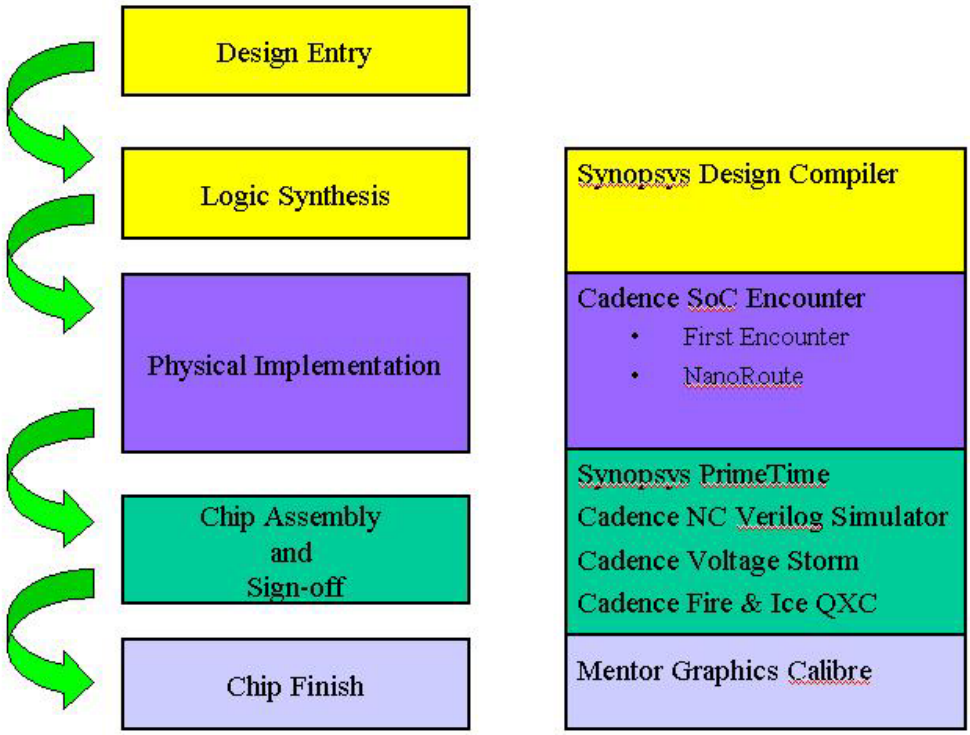

Figure 1: HeJian Reference Design Flow

Design Tools used in HeJian's Reference Design:

Logic Synthesis

Logic synthesis is done by using Synopsys Design Compiler™ (DC-Shell). HDL (Hardware Description Language) is used to describe the functionality of a design. The functionality of the design could be in different abstraction levels (Behavioral, Register-Transfer-Level/RTL, or Gate Level) and using different syntax format (Verilog or VHDL).

Physical Implementation

Once the gate level representation of the design has been created, you will perform physical implementation of the design using Cadence SoC Encounter. SoC Encounter can convert gate-level representation of the design to GDSII representation.

RC Extraction

Cadence Fire & Ice QXC™ is industry's most accurate sign-off extractor that takes into account on-die process variations resulting from optical and copper manufacturing effects at 180nm.

Power Sign Off

Cadence VoltageStorm™ is the leading power grid verification solution. You can perform power analysis using VoltageStorm to check IR, RJ, and RC.

Static Timing Sign Off

After physical implementation, you will need to analyze static timing information with Synopsys PrimeTime™. You can validate the timing performance of a design by checking all possible paths for timing violations.

Dynamic Functional Timing Sign Off

After checking static timing information, you will need to check for the functional simulation by using Cadence NC-Verilog Simulator™. You can verify the functional correctness between the pre-layout simulation v.s. post-layout simulation.

Physical Verification

After completing the layout design, you will perform physical verification including DRC (Design Rule Check) and LVS (Layout Versus Schematic). In physical verification step, you will use Calibre from Mentor Graphics to check all design rules. If the design contains no violations, then it is ready to generate mask and fabricate

chip. Otherwise if violations are found, you will have to adjust them and then go back to the layout design step.

To learn more: Find out more about how EE Solutions and HeJian are partnering to fulfill your design needs by visiting:

http://www.hjtc.com.cn
http://www.e2-solutions.com.tw