Free-of-Charge Libraries

Virtual Silicon 0.25um Library

Standard Cells

- 500+ high performance standard cells
- 11-track cell architecture, performance optimized for 150~400 MHz
- Average cell density of 45K gates/sq.mm
- Multiple drive strengths
- Hand-crafted layout
- Scan version of every flip-flop available
- Fully contacted well ties
- Accurate modeling and characterization for timing and power

Inline I/O

- 70+ 3.3V I/O pads
- Pad pitch: 60um
- Multiple current drives up to 24mA
- Input buffer types - Pull-up/pull-down resistor, pad keeper, clock driver and normal/Schmitt
- Output and bi-directional buffer types with slew rate control
- Silicon proven ESD and latch-up structures

Two Port Register File

- Synchronous reads/writes
- Static design with zero standby current
- Automated EDA views
- Routable over the core with higher metal layer

Architecture	Word	Bit	Mux	Size	Access Time (ns)
Two Port Register	8 - 256 (Increment: 2X mux)	4 - 72 (Increment: 2)	NA	32 bit - 18 Kbit	128 x 64 Typical: 1.37 Worst: 2.48

HEJIAN

Faraday 0.25um Library

Standard Cells

- 400+ high performance standard cells
- 8-track cell architecture
- Average cell density >60K gates/sq.mm
- Optimized multiple drive strengths
- High porosity and routability
- Scan version of every flip-flop available
- Ultra low power cell available
- Gated input for preventing leakage
- Fully tool models support

Inline and Staggered I/O

- 2.5V, 3.3V I/O pads
- 2.5V/3.3VT, 3.3V/5VT I/O pads
- Support over 500+ IO Functions
- Pad pitch: 65um (In-line), 40um (Stagger)
- Programmable current drives and slew rate control from 2mA to 16mA
- Programmable pull-up/pull-down resistor, normal/ Schmitt trigger
- Provide 90+ programming features in one I/O pad
- In-line to staggered I/O corner available

Single Port SRAM, Two Port SRAM, Diffusion and Via2 ROM Compilers

- Synchronous reads/writes
- Static design with zero standby current
- Byte write capability
- Provides both high speed and low power SRAMs
- Ability to compile to multiple aspect ratio
- Scan and BIST support
- Power port connections support
- Zero hold time for inputs

Architecture	Word	Bit	Mux	Size	Access Time (ns)
Single Port Sync. SRAM	4 - 64K (Increment:2X mux)	1 - 128 (Increment: 1)	1, 2, 4, 8, 16	4 bit - 512Kbit	4K x 16 Typical: 1.9 Worst: 3.1
Two Port Sync. SRAM	4 - 16K (Increment:2X mux)	1 - 80 (Increment: 1)	1, 2, 4, 8	4 bit - 160 Kbit	4K x 16 Typical: 2.1 Worst: 3.3
Via2 ROM	128 - 64K (Increment:128X mux)	2 - 128 (Increment: 1)	1, 2, 4, 8	256 bit - 1 Mbit	4K x 16 Typical: 3.3 Worst: 5.5
Diffusion ROM	128 - 64K (Increment:128X mux)	2 - 128 (Increment: 1)	1, 2, 4, 8	256 bit - 1 Mbit	4K x 16 Typical: 7.3 Worst: 12.1